20.6 A Fully Integrated 2.4GHz IEEE 802.15.4 Compliant Transceiver for ZigBee Applications

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This single-chip RF transceiver provides a complete radio interface between the antenna and the microcontroller. It comprises the analog radio block, digital demodulation including time and frequency synchronization and data buffering. The number of external components is minimized so that only a crystal and 3 decoupling capacitors are required. The bidirectional differential antenna pins are commonly used for RX and TX, therefore, no external antenna switch is needed. Two on-chip low-drop voltage regulators provide the analog and digital 1.8V supply. The SPI interface and the control registers are implemented in 0.36µm technology for data retention in sleep mode when voltage regulators are turned off. The RX and TX signal processing part is implemented using 0.18µm libraries, utilizing the low power consumption and the high density of the technology. The IC is implemented in a 1P 6M 0.18µm CMOS technology with MIM capacitors.

The transceiver block diagram is shown in Fig. 20.6.1. The receiver path is based on a low-IF topology. The channel filter consists of three single side-band active RC resonators forming a 2MHz bandpass filter with Butterworth characteristic centered at 2MHz. Two 1st-order highpass filters are added to the signal path to achieve capacitive coupling at the single side-band filter (SSBF) output to suppress dc offset and integrator feedback at the limiter amplifier. The resulting frequency response is shown in Fig. 20.6.2. The 3-stage limiter amplifier provides sufficient gain to overcome the dc offset of the succeeding single-channel ADC, and generates a digital RSSI signal with 3dB granularity. The low-IF signal sampled at 16MHz with 1b resolution is applied to the digital signal processing part.

Much attention is paid to circuit blocks running at 2.4GHz to minimize power consumption. The RF front-end only uses a single LO signal. Hence, there is no power consumption needed for generating and buffering the LO Q-signal. Therefore, the received signal is split into I and Q components utilizing a passive 2-stage poly-phase filter (PPF). As the mixer is also passively implemented using commutating analog switches, the only power consuming block of the RX RF front-end is the LNA. To compensate the losses of the PPF and the mixer, the LNA gain has to be increased. This is accomplished by stacking 2 amplifier stages sharing the same bias current as shown in Fig. 20.6.3. The LNA input stage is a common-gate configuration. This simplifies input matching as the transistor transconductance is set to $g_m = 1/(50\Omega)$. Furthermore, it features lower input parasitic capacitances compared to a gate input which is important as the PA parasitic capacitances are also connected to the LNA input nodes. The LNA provides 32dB voltage gain including the PPF load.

A differential RF input is chosen to provide common-mode rejection suppressing switching noise of the digital signal processing block. As the common-gate input stage exhibits no common-mode rejection, the rejection is achieved by the resonance tank load. The resonance tank is built of a symmetrical 20nH inductor with a central tap. As both parts of the coil have magnetic coupling, the differential inductance is higher than the common-mode inductance. Hence, the common-mode resonance peak is shifted to higher frequencies, leading to a lower common-mode gain at the desired frequency compared to the differential gain. Differential resonance capacitors enhance the common-mode rejection but the effect is small as most of the resonance capacitance is single-ended, stemming from device and layout parasitic capacitances.

The second LNA stage is a cascode configuration to mitigate Miller capacitance feedback as it would be seen using a single transistor stage. Bias voltage vbn2 is adjusted in a way such that both transistors M1p/n and M21p/n have the same drain-source voltage. A constant-g_m bias current source determines the bias voltage vbn1 and sets the LNA bias current to 2.4mA. The measured common-mode rejection is shown in Fig. 20.6.4. Within the ISM band frequency range the common mode rejection is greater than 40dB.

In transmit mode, the LNA is turned off by transistor M0. The PA common-mode bias voltage is regulated to half the supply voltage (0.9V) by a feedback loop. This is needed as the PA is built as a push-pull differential amplifier exploiting the power efficiency of this topology. Furthermore, a slew-rate control is implemented to ramp up the transmit power within approximately 1µs. An important feature of the 2-stage PA is the isolation when turned off, as there is a direct path from the LO signal to the antenna. More than 70dB isolation is achieved by inserting analog switches, reducing the buffer gain in the off-state.

A digital AGC is implemented to cover the 94dBm input-signal dynamic range from -102dBm to -8dBm. The RSSI signal of the limiter amplifier is used by the AGC state machine to reduce gain by two gain steps of 24dB each. The first gain step is realized in the LNA to increase large-signal robustness. The second gain step is shared between the LNA and the SSBF. To ensure stability of the digital gain control loop, a 6dB hysteresis is implemented. The AGC updates receiver gain within a 2µs raster so that the maximum settling time for 2 gain steps is less than 5µs. As the preamble is 128µs long, there is sufficient time left for preamble detection and synchronization.

Direct VCO modulation is used to generate the transmit signal. The modulation scheme is offset-QPSK (O-QPSK) with 32-chip spreading codes, which is identical to minimum shift keying (MSK) modulation when translating the code sequences. The modulation signal is applied to both the VCO and the fractional-N PLL to ensure the coherent phase modulation required for demodulation as an O-QPSK signal. The TX spectrum is shown in Fig. 20.6.5.

Measurement results are summarized in Fig. 20.6.6. In conjunction with the digital demodulator, the receiver sensitivity is -101dBm for 1% packet error rate defined in the IEEE 802.15.4 standard. The transceiver chip consumes 44mW and 47mW in receive and transmit mode, respectively, when running at 3V supply. A micrograph of the 5.77mm^2 die is shown in Fig. 20.6.7. The core dimensions are 1.85mm×2.05mm, leading to 66% die-size utilization. To enhance the utilization, both voltage regulators and the crystal oscillator are located in the pad ring area.

References:

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[2] M.S.J. Steyaert, et al., "Low-Voltage Low-Power CMOS_RF Transceiver Design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 873-887, Jan., 2002.

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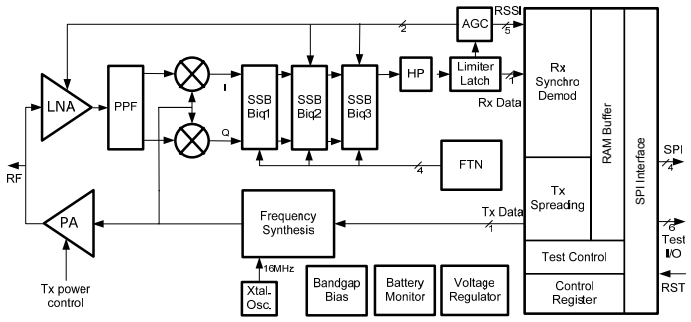

Figure 20.6.1: Transceiver block diagram.

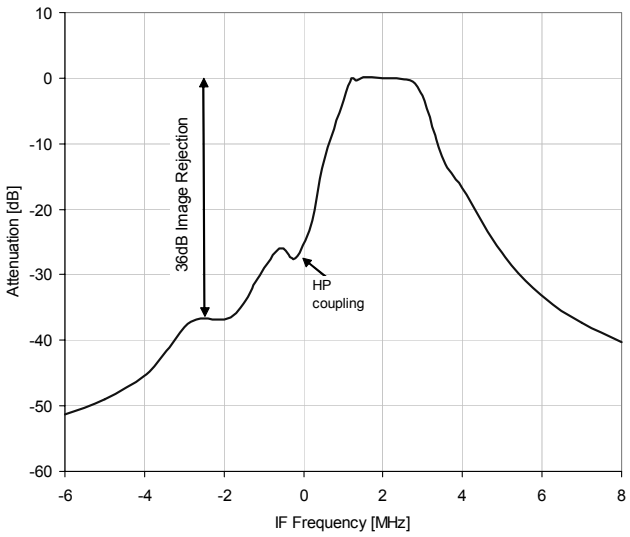

Figure 20.6.2: Receiver frequency characteristic.

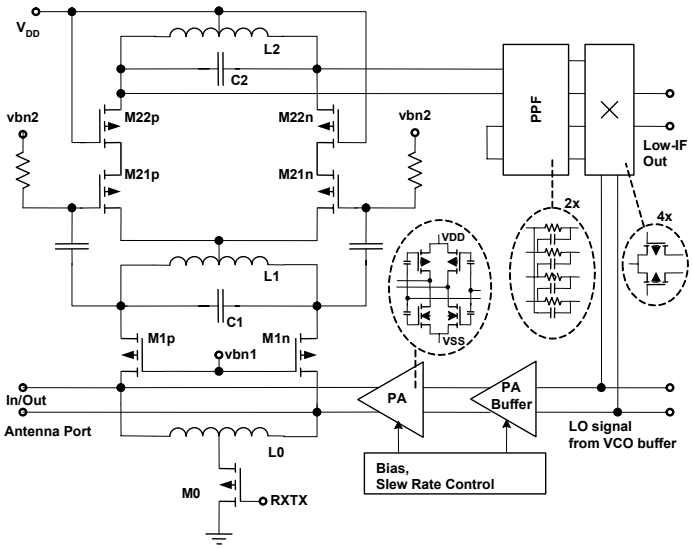

Figure 20.6.3: LNA and RF front-end schematic.

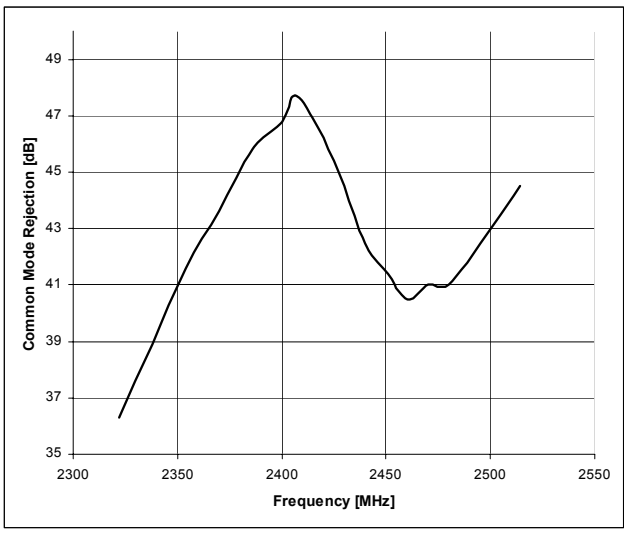

Figure 20.6.4: Measured common-mode rejection.

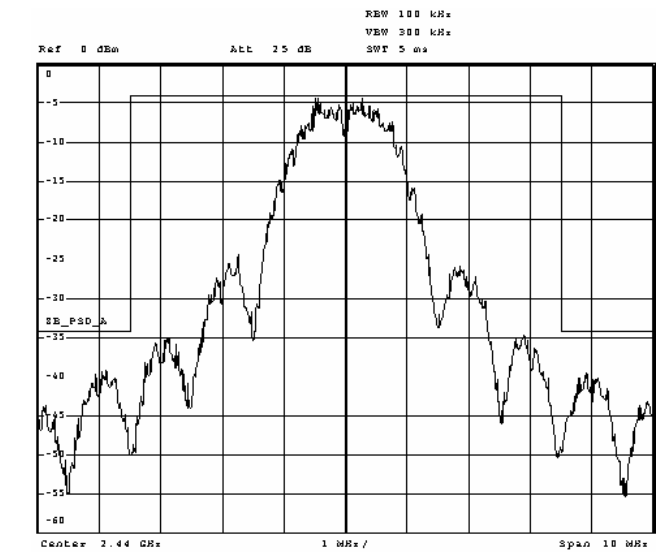

Figure 20.6.5: TX spectrum with O-QPSK modulation.

Receiver/Transmitter		Current Consumption [mA]		
NF	5.7dB	Supply Volt.	1.8-3.75V	
IP3	-16dBm		**Rx**	**Tx**
Rx sensitivity	-102dBm	Analog	5.6	7.5
LO Leak.	<-76dBm	Digital	3.7	2.8
Tx power	3dBm	PLL	5.4	5.4
Image Reject.	36dB	**Total**	**14.7**	**15.7**
CM Rejection	>40dB			

Figure 20.6.6: Measurement results.

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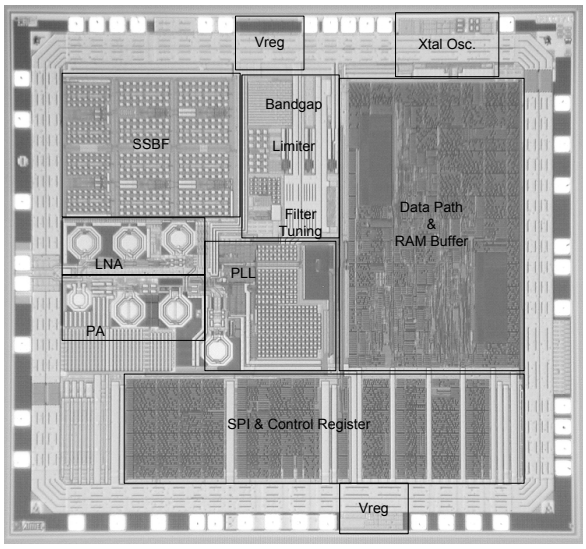

Figure 20.6.7: Die micrograph.

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